Code.No: **R05310201** | R05 | SET-1

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
COMPUTER ORGANIZATION
(COMMON TO EEE, ECE, EIE, E.CON.E, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1. Write the RTL Codes for various addressing models and explain with examples. [16]

2. Micro-program Sequencer is to present address to Control Memory. In this process, explain the role of Micro-program Sequencer with the help of diagram. [16]

3. With the help of a flow Chart, explain the addition and subtraction for signed 2's compliment data. [16]

4. How the Associative Memory is mapped? Explain with diagram and example. [16]

5. Explain various Interrupt – Initiated I/O methods for data transfer. Give a brief sketch of Daisy Chaining Priority. [16]

6. Draw the Flow chart for point addition and subtraction for pipeline operations. Explain with an example. [16]

7.a) Explain about Inter-processor Communication.
b) Do the binary operations using 2's complement for the following problems. [8+8]

i) – 23 ii) + 15
(+) + 45 (–) – 27

8. Write short notes on:
a) Error detection Codes
b) RISC processor
c) DMA
d) Array Processors. [16]

--ooOoo—

Code.No: **R05310201** | R05 | SET-2

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
COMPUTER ORGANIZATION
(COMMON TO EEE, ECE, EIE, E.CON.E, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1. With the help of a flow Chart, explain the addition and subtraction for signed 2's compliment data. [16]

2. How the Associative Memory is mapped? Explain with diagram and example. [16]

3. Explain various Interrupt – Initiated I/O methods for data transfer. Give a brief sketch of Daisy Chaining Priority. [16]

4. Draw the Flow chart for point addition and subtraction for pipeline operations. Explain with an example. [16]

5.a) Explain about Inter-processor Communication.
b) Do the binary operations using 2's complement for the following problems. [8+8]

i)		– 23	ii)	+ 15
(+)		+ 45	(–)	– 27

6. Write short notes on:
a) Error detection Codes
b) RISC processor
c) DMA
d) Array Processors. [16]

7. Write the RTL Codes for various addressing models and explain with examples. [16]

8. Micro-program Sequencer is to present address to Control Memory. In this process, explain the role of Micro-program Sequencer with the help of diagram. [16]

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Code.No: **R05310201** | R05 | SET-3

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
COMPUTER ORGANIZATION
(COMMON TO EEE, ECE, EIE, E.CON.E, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1. Explain various Interrupt – Initiated I/O methods for data transfer. Give a brief sketch of Daisy Chaining Priority. [16]

2. Draw the Flow chart for point addition and subtraction for pipeline operations. Explain with an example. [16]

3.a) Explain about Inter-processor Communication.
b) Do the binary operations using 2's complement for the following problems. [8+8]

i) – 23 (+) + 45

ii) + 15 (–) – 27

4. Write short notes on:
a) Error detection Codes
b) RISC processor
c) DMA
d) Array Processors. [16]

5. Write the RTL Codes for various addressing models and explain with examples. [16]

6. Micro-program Sequencer is to present address to Control Memory. In this process, explain the role of Micro-program Sequencer with the help of diagram. [16]

7. With the help of a flow Chart, explain the addition and subtraction for signed 2's compliment data. [16]

8. How the Associative Memory is mapped? Explain with diagram and example. [16]

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Code.No: **R05310201** | **R05** | **SET-4**

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
COMPUTER ORGANIZATION
(COMMON TO EEE, ECE, EIE, E.CON.E, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) Explain about Inter-processor Communication.
b) Do the binary operations using 2's complement for the following problems. [8+8]

i) – 23 (+) + 45

ii) + 15 (–) – 27

2. Write short notes on:
a) Error detection Codes
b) RISC processor
c) DMA
d) Array Processors. [16]

3. Write the RTL Codes for various addressing models and explain with examples. [16]

4. Micro-program Sequencer is to present address to Control Memory. In this process, explain the role of Micro-program Sequencer with the help of diagram. [16]

5. With the help of a flow Chart, explain the addition and subtraction for signed 2's compliment data. [16]

6. How the Associative Memory is mapped? Explain with diagram and example. [16]

7. Explain various Interrupt – Initiated I/O methods for data transfer. Give a brief sketch of Daisy Chaining Priority. [16]

8. Draw the Flow chart for point addition and subtraction for pipeline operations. Explain with an example. [16]

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